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1 RF circuit design and design methodology: A 1GHz CMOS fourth-order continuous-time bandpass sigma delta modulator for RF receiver front end A/D conversion

K. Praveen Jayakar Thomas, Ram Singh Rana, Yong Lian

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(661.92 KB) Additional Information: full citation, abstract, references

A design and circuit implementation of a CMOS fourth-order continuous-time bandpass *fs*/4 sigma delta modulator is presented. The fully differential architecture of the modulator includes integrated LC resonators with active Q enhancement and return to zero, half return to zero latches to drive the feedback switched current source DACs. The modulator, designed for 0.18µm/1.8V 1P6M CMOS process occupies a total area of 1.8mm^2 dissipating 290mW from a 1.8V power supp ...

2 Mixed analog-digital design: On the dynamic behavior of a novel digital-only sigma--delta A/D converter

Marcel Jacomet, Josef Goette, Venanz Zbinden, Christian Narvaez

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Publisher: ACM Press

Full text available: pdf(293.94 KB) Additional Information: full citation, abstract, references, index terms

Conventional sigma-delta (ΣΔ) analog-to-digital (Ad) converters are based on an analog ΣΔ modulator followed by a digital filter. In this paper we propose a new architecture of a first-order ΣΔ modulator that needs *no active* analog components. We call this ΣΔ modulator "digital-only," and implement with it Ad converters in Fpga's or directly in the software of microprocessors. We here discuss aspects of the dynamic behavio ...

Keywords: ΣΔ modulator, A/D converter, FPGA

3 Circuits for low power wireless: A novel continuous-time common-mode feedback for low-voltage switched-OPAMP

M. Ali-Bakhshian, K. Sadeghi

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(572.94 KB) Additional Information: full citation, abstract, references, index terms

A novel rail-to-rail and fast continuous-time common-mode feedback (CMFB) strategy is presented proper for low-voltage Switched-OPAMP (SO) circuits. The threshold voltage change due to bulk signal is used to measure the output voltage. To satisfy speed requirements, averaging common-mode (CM) level and amplifying error signal are realized in a single block. Finally, the measured CM level is controlled by applying an error-voltage dependent current to the output nodes. As a design example, a modi ...

Keywords: CMFB, continuous-time, delta-sigma, low-voltage, switched-OPAMP

4 A Methodology for Designing Continuous-Time Sigma-Delta Modulators

Philippe Benabes, Mansour Keramat, Richard Kielbasa

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(534.46 KB) Publisher Site Additional Information: full citation, abstract

A methodology for analysis and synthesis of lowpass sigma-delta (/spl Sigma//spl Delta/) converters is presented in this paper. This method permits to synthesize /spl Sigma//spl Delta/ modulators employing continuous-time filters from discrete-time topologies. The analysis method is based on the discretization of continuous-time model and using a discrete simulator which is more efficient than an analog simulator. Finally, a realistic design of a second-order /spl Sigma//spl Delta/ modulator wit ...

Keywords: sigma-delta modulation, design methodology, continuous-time sigma-delta modulator, continuous-time filter, discrete-time topology, discrete simulation, low-pass second-order /spl Sigma//spl Delta/ modulator, compensation, DAC

5 A design strategy for low-voltage low-power continuous-time sigma-delta A/D converters

F. Gerfers, Y. Manoli

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Press

Full text available: pdf(619.81 KB) Additional Information: full citation, references, citings, index terms

6 Frontmatter (TOC, Letters, Election results, Software Reliability Resources!, Computing Curricula 2004 and the Software Engineering Volume SE2004, Software Reuse Research, ICSE 2005 Forward)

July 2005 **ACM SIGSOFT Software Engineering Notes**, Volume 30 Issue 4

Publisher: ACM Press

Full text available: pdf(6.19 MB) Additional Information: full citation, index terms

7 Analog design for reuse - case study: very low-voltage sigma-delta modulator

M. Dessouky, A. Kaiser, M. Louërat, A. Greiner

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Press

Full text available: pdf(360.20 KB) Additional Information: full citation, references, index terms

8 Denial-of-service: Robustness to inflated subscription in multicast congestion control

Sergey Gorinsky, Sugat Jain, Harrick Vin, Yongguang Zhang
August 2003 **Proceedings of the 2003 conference on Applications, technologies, architectures, and protocols for computer communications**
Publisher: ACM Press

Full text available: pdf(282.59 KB) Additional Information: full citation, abstract, references, citings, index terms

Group subscription is a useful mechanism for multicast congestion control: RLM, RLC, FLID-DL, and WEBRC form a promising line of multi-group protocols where receivers provide no feedback to the sender but control congestion via group membership regulation. Unfortunately, the group subscription mechanism also offers receivers an opportunity to elicit self-beneficial bandwidth allocations. In particular, a misbehaving receiver can ignoreguidelines for group subscription and choose an un ...

Keywords: congestion control, fair bandwidth allocation, misbehaving receivers, multicast, robustness

9 Power consumption reduction in high-speed ΣΔ bandpass modulators

P. Cusinato, F. Stefani, A. Baschirotto
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Publisher: ACM Press

Full text available: pdf(1.20 MB) Additional Information: full citation, abstract, references, index terms

Power consumption is a key point in the design of high-speed switched capacitor (SC) circuits, which allow to efficiently implement a number of analog functions. Among them, SC &Sgr;&Dgr; modulators are very popular for A/D conversion: in this kind of circuits, operational amplifiers are the most consuming cells because of their requirements in terms of DC gain and unity-gain frequency. A new amplifier with 110dB DC gain and a unity-gain frequency of 250MHz is presented. The large power con ...

10 Low-voltage low-power switched-current circuits and systems

Nianxiong Tan, S. Eriksson
March 1995 **Proceedings of the 1995 European conference on Design and Test**
Publisher: IEEE Computer Society

Full text available: pdf(642.50 KB) Publisher Site Additional Information: full citation, abstract, citings

This paper presents low-voltage low-power switched-current circuits and systems. Novel class AB configuration and common-mode feedforward are the essence. A delay line, memory cell, oversampling A/D converter, and chopper-stabilized oversampling A/D converter were designed and implemented. Measurement results are presented as well.

Keywords: CMOS IC, CMOS analogue integrated circuits, LV switched-current circuits, SI memory cell, analogue processing circuits, analogue storage, analogue-digital conversion, chopper-stabilized oversampling ADC, class AB configuration, common-mode feedforward, delay line, delay lines, feedforward, low-power switched-current circuits, oversampling A/D converter, sampled data circuits, switched current circuits

11 Automatic Synthesis and Simulation of Continuous-Time [Sigma-Delta] Modulators

H. Aboushady, L. de Lamarre, N. Beilleau, M. M. Louërat
February 2004 **Proceedings of the conference on Design, automation and test in**

Europe - Volume 1
Publisher: IEEE Computer Society
Full text available: pdf(253.26 KB) Additional Information: full citation, abstract, index terms

This paper presents a mixed equation-based and simulation-based design methodology for continuous-time Sigma-Delta modulators from high level specifications down to Layout. The calculation and scaling of the Sigma-Delta coef.cients as well as circuit sizing and layout generation are implemented in the same analog design environment CAIRO+. The design of a complete third order current-mode continuous-time Sigma-Delta modulator is taken as an example to show the effectiveness of the proposed desig ...

12 A two-layer library-based approach to synthesis of analog systems from VHDL-AMS specifications
Alex Doboli, Nagu Dhanwada, Adrian Nunez-Aldana, Ranga Vemuri
April 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 2
Publisher: ACM Press
Full text available: pdf(658.00 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a synthesis methodology for analog systems described using VHDL-AMS language. Synthesis produces net-lists of analog components that are selected from a library, and sized so that specified objectives (like AC response, signal to noise ratio, dynamic range, area) are optimized. The gap between abstract specifications and implementations is bridged using a two-layered methodology. The first layer is architecture generation. The second layer is component synthesis and constrain ...

Keywords: Analog synthesis, VHDL-AMS, branch-and-bound, genetic algorithms, performance estimation

13 On the optimum design of regulated cascode operational transconductance amplifiers
Thomas Burger, Qiuting Huang
August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(710.23 KB) Additional Information: full citation, abstract, references, index terms

An optimal design procedure to achieve minimum power consumption for a given technology and gain bandwidth is presented. Regulated cascode gain enhancement is used to ensure sufficient DC-gain at minimum gate length transistors. To validate the approach five folded cascode OTA's have been implemented, spanning a bias range of 1μA - 10mA, with measured unity-gain bandwidths within 20% of the designed value. For 17 mW at 3 V, a 0.5 μm

14 High speed converters, amplifiers, and low power analog circuits: A 1-V 1-mW high-speed class AB operational amplifier for high-speed low power pipelined A/D converters using "Slew Boost" technique
H. A. Aslanzadeh, S. Mehrmanesh, M. B. Vahidfar, A. Q. Safarian, R. Lotfi
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(267.44 KB) Additional Information: full citation, abstract, references, index terms

An ultra-low-voltage low-power high-speed class-AB operational amplifier with a new structure is presented. A new technique called "Slew Boost" is introduced to improve amplifier's large-signal settling behavior, most useful in switched-capacitor circuits such as pipelined ADCs, sigma delta modulators, etc. The proposed op-amp has been designed

to be employed in the first stage of a 10bit 150MSamples/sec pipelined analog-to-digital converter. Simulation results of the proposed fully-differential ...

Keywords: CMOS analog circuit, Slew Boost technique, class AB, high speed, low power, operational amplifier, pipelined analog to digital converter, ultra low voltage

15 Proceedings of the SIGNUM conference on the programming environment for development of numerical software

March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1

Publisher: ACM Press

Full text available: pdf(5.02 MB) Additional Information: full citation

16 A 1.5V low-power third order continuous-time lowpass ΣΔ A/D converter (poster session)

Friedel Gerfers, Yiannos Manoli

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(222.84 KB) Additional Information: full citation, abstract, references, index terms

This paper presents the design of a 3rd-order lowpass &Sgr;&Dgr; g-to-digital (A/D) converter using a continuous-time(CT) loopfilter. The loopfilter has been implemented by using active RC-integrators. The influence of the low supply voltage on the building blocks such as the amplifier and the common mode feedback as well as on the overall &Sgr;&Dgr modulator is discussed. Simulation results of the 1.5V CT &Sgr;&Dgr; A/D converter show a 75 dB dynamic range in a bandwidth of ...

17 Session 9: Oversampled gain-boosting

Omid Oliaei

August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(194.94 KB) Additional Information: full citation, abstract, references, index terms

A dynamic gain-enhancement technique suitable for lowvoltage low-power oversampling circuits, particularly sigma-delta converters, is presented. This method makes use of a discrete time integrator to improve gradually the output resistance of the main amplifier over successive clocks.

Keywords: ADC, DAC, MOS amplifier, OTA, bootstrapping, gain boosting, gain enhancement, sigma-delta, switched-capacitor

18 Noise considerations for mixed-signal RF IC transceivers

Sayfe Kiaei, David Allstot, Ken Hansen, Nishath K. Verghese

January 1998 **Wireless Networks**, Volume 4 Issue 1

Publisher: Kluwer Academic Publishers

Full text available: pdf(629.05 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses design trade-offs for mixed-signal radio frequency integrated circuit (RF IC) transceivers for wireless applications in terms of noise, signal power, receiver linearity, and gain. During air wave transmission, the signal is corrupted by channel noise, adjacent interfering users, image signals, and multi-path fading. Furthermore, the

receiver corrupts the incoming signal due to RF circuit non-linearity (intermodulation), electronic device noise, and digital switching noi ...

19 High speed converters, amplifiers, and low power analog circuits: A low-power design methodology for high-resolution pipelined analog-to-digital converters

Reza Lotfi, Mohammad Taherzadeh-Sani, M. Yaser Azizi, Omid Shoaei

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(269.36 KB) Additional Information: full citation, abstract, references, index terms

In this paper a general method to design a pipelined ADC with minimum power consumption is presented. By expressing the total static power consumption and the total input-referred noise of the converter as functions of the capacitor values and the resolutions of the converter stages, a simple optimization algorithm is employed to calculate the optimum values of these parameters, which lead to minimum power consumption while a specified noise requirement is satisfied. To determine the bias curren ...

Keywords: low-power design, operational amplifiers, pipelined analog-to-digital converters

20 Two-dimensional position deteciton system with MEMS accelerometer for MOUSE applications

Seungbae Lee, Gi-Joon Nam, Junseok Chae, Hanseup Kim, Alan J. Drake

June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(1.40 MB) Additional Information: full citation, abstract, references, index terms

A hybrid two-dimensional position sensing system is designed for mouse applications. The system measures the acceleration of hand-movements which are converted into two-dimensional location coor-dinates. The system consists of four major components: 1) MEMS accelerometers, 2) CMOS analog read-out circuitry, 3) an accelera-tion magnitude extraction module, and 4) a 16-bit RISC micropro-cessor. Mechanical and analog circuit simulation shows that the designed padless mouse system can detect a ...

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Aboushady, H.; Louerat, M.-M.;
Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE Internatio on
Volume 2, 2-5 Sept. 2001 Page(s):963 - 966 vol.2
Digital Object Identifier 10.1109/ICECS.2001.957633
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Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEE Symposium on
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Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd An
Volume 1, 23-27 June 2002 Page(s):50 - 54 vol.1
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Shuenn-Yuh Lee; Chih-Jen Cheng;
Circuits and Systems, 2004. Proceedings. The 2004 IEEE Asia-Pacific Confere
Volume 1, 6-9 Dec. 2004 Page(s):41 - 44 vol.1
Digital Object Identifier 10.1109/APCCAS.2004.1412686
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Punzenberger, M.; Enz, C.;

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VLSI Technology, Systems, and Applications, 1995. Proceedings of Technical International Symposium on
31 May-2 June 1995 Page(s):365 - 369
Digital Object Identifier 10.1109/VTSA.1995.524721

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7. **A CMOS smart temperature sensor with a 3/spl sigma/ inaccuracy of /spl deg/C from -55/spl deg/C to 125/spl deg/C**
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Solid-State Circuits, IEEE Journal of
Volume 40, Issue 12, Dec. 2005 Page(s):2805 - 2815
Digital Object Identifier 10.1109/JSSC.2005.858476

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Hirota, A.; Nagai, S.; Nakaoka, M.;
Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Ani
Volume 2, 23-27 June 2002 Page(s):682 - 686 vol.2
Digital Object Identifier 10.1109/PSEC.2002.1022532

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Guo-Ming Sung; Kuo-Hsuan Chang; Wen-Sheng Lin;
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23-26 May 2005 Page(s):5573 - 5576 Vol. 6
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Digital Object Identifier 10.1109/ICECS.2001.957556

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Volume 3, 5-8 Sept. 1999 Page(s):1515 - 1518 vol.3
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☐ **15. A current-mode continuous-time ΣΔ modulator with delayed return-to-ze**
Aboushady, H.; Mendes, E.deL.; Dessouky, M.; Loumeau, P.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE Interna on
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Mertens, A.; Eckardt, D.;
Industry Applications, IEEE Transactions on
Volume 34, Issue 5, Sept.-Oct. 1998 Page(s):1139 - 1146
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Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G Devices and Systems]
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Hirano, S.; Hasegawa, H.; Nagasawa, S.; Kato, S.; Miyahara, K.; Enomoto, Y.;
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Volume 13, Issue 2, Part 1, June 2003 Page(s):488 - 491
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Volume 1, 14-17 Aug. 2001 Page(s):247 - 250 vol.1
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Lindfors, S.;
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Digital Object Identifier 10.1109/ICECS.2000.911500
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Oliaei, O.; Aboushady, H.;
Electronics, Circuits and Systems, 1998 IEEE International Conference on
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Harris, F.; McKnight, B.; Constantinides, T.;
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Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G
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AbstractPlus | Full Text: PDF(570 KB) **IEE JNL**

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Naiknaware, R.; Fiez, T.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE Interna
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Volume 2, 30 May-2 June 1999 Page(s):33 - 36 vol.2
Digital Object Identifier 10.1109/ISCAS.1999.780612

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Results for "((sigma <in>metadata) <and> (delta <in>metadata))<and> (source<in..." e-mail
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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	2	"6507301" noise	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/29 09:31
L3	0	"6507301".pn. noise	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/29 09:31
L4	2	"6507301".pn. capacitor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/29 09:31
L6	8	("4509037"|"4737702"|"4998109"|"5227795").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/29 10:03
S1	0	continous delta sigma current source falling	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/23 10:50
S2	1	(continuous or continuously) delta sigma current source fall$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/23 13:43
S3	2	"4509037".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/23 10:57
S4	2	"4998109".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/23 10:57

EAST Search History

S5	9	(continuous or continuously) delta sigma current source	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/23 11:07
S6	3	delta sigma current source integrat$ quantiz$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 09:55
S7	5	"6507301"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/29 09:25
S8	2	"6507301".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/23 11:19
S9	1	"6507301".pn. and (continuous or continuously)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/23 12:56
S10	359	(continuous or continuously) delta sigma	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/23 13:43
S11	186	(continuous or continuously) NEAR4 delta sigma	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/23 13:45
S12	15	(continuous or continuously) NEAR4 delta sigma same (integrat$ quantiz$)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/23 14:30

EAST Search History

S13	2	(continuous or continuously) NEAR4 delta sigma same (integrat$ quantiz$)current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/23 14:30
S14	2	"6507301".pn. current	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/24 10:07
S15	13	delta sigma current source feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 10:10
S16	0	"6507301".pn. clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 12:27
S17	0	"6507301".pn. timing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/24 10:14
S18	1	"6507301".pn. period	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/24 10:08
S19	90	delta sigma current feedback	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 10:10
S20	77	delta sigma current feedback not S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 10:10

EAST Search History

S21	0	delta sigma current clock feedback not S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 10:11
S22	2	delta sigma current period feedback not S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 10:19
S23	1	"6507301".pn. resistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/24 10:14
S24	77	delta sigma current feedback not S15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 11:41
S25	9	delta sigma current source dac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 11:50
S26	32	delta sigma same current source dac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 11:50
S27	23	delta sigma same current source dac not S25	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 11:55
S28	0	delta NEAR1 sigma same feeback current dac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 11:56

EAST Search History

S29	18	delta NEAR1 sigma same feedback current dac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 12:07
S30	8	("4509037"|"4737702"|"4998109"|"5227795").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/24 12:08
S31	4	("4509037"|"4737702"|"4998109"|"5227795").PN.	USPAT	AND	ON	2006/03/24 12:12
S32	6	voltage current source (digital ADJ1 analog or da or dac) and sigma.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 12:20
S33	28	voltage current source (digital ADJ1 analog or da or dac) and sigma ADJ1 delta	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 12:20
S34	23	voltage current source (digital ADJ1 analog or da or dac) and sigma ADJ1 delta not S32	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 12:26
S35	138	voltage controlled current source (digital ADJ1 analog or da or dac)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 12:25
S36	5	voltage current controlled source (digital ADJ1 analog or da or dac) and sigma ADJ1 delta	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/24 12:27
S37	32	voltage current controlled source (digital ADJ1 analog or da or dac) and sigma near1 delta	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/03/27 08:57

EAST Search History

S38	5	voltage current controlled source (digital ADJ1 analog or da or dac) and sigma near1 delta	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 09:01
S39	138	voltage current controlled source (digital ADJ1 analog or da or dac)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 09:02
S40	25	voltage current controlled source (digital ADJ1 analog or da or dac) and "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 09:45
S41	725	current source (digital ADJ1 analog or da or dac) and "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 09:45
S42	657	current NEAR1 source (digital ADJ1 analog or da or dac) and "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 09:46
S43	158	current NEAR1 source (digital ADJ1 analog or da or dac) and delta and "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 09:47
S44	135	current NEAR1 source (digital ADJ1 analog or da or dac) and delta and sigma and "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 09:47
S45	135	current NEAR1 source (digital ADJ1 analog or da or dac) and delta NEAR1 sigma and "341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/03/27 10:57
S46	5281	(341/143,155,144,118,120,156, 158).CCLS.	USPAT	OR	OFF	2006/03/29 09:51

EAST Search History

S47	1	"6507301".pn. continuous	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 13:21
S48	1	"6507301".pn. discharging	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 13:22
S49	0	"6507301".pn. time	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 13:22
S50	0	"6507301".pn. clock$	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 13:23
S51	1	"10/530,762"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 14:30
S52	1	"10/530,762" and "gm"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 14:33
S53	434	"gm-c"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 14:36
S54	4414	resistance NEAR2 mass	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/03/28 14:36